## ABSTRACT OF THE DISCLOSURE

An integrated semiconductor memory, and method for operating such a memory, in particular a DRAM memory, having local data lines (LDQT, LDQC) segmented in the column direction (Y), which local data lines can be connected by a CSL switch in response to a column select signal fed via a CSL line (CSL) running in the row direction (X) to primary sense amplifiers for transferring or accepting spread data signals to or from bit lines of the respective segment (I, II, III), LDQ switches are arranged at the interfaces between adjacent segments of the local data lines (LDQT, LDQC) for their connection to the local data lines (LDQT, LDQC) of adjacent segments (I, II, III). LDQ switches, depending on a control signal fed separately to each of said LDQ switches, are closed during a precharge phase, which takes place before each read cycle, of at least two adjacent LDQ segments.


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